A single-chip 24 GHz receiver front-end using a commercially available SiGe HBT foundry process

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***Abstract* — The authors have demonstrated a fully integrated receive frontend addressing the ISM-Band at 24 GHz utilizing a standard SiGe HBT MMIC process with a relaxed emitter scaling of 1.2 μm, for the first time. Extremely compact circuit design and layout techniques are applied to a mature Si/SiGe technology, resulting in a low-cost integrated circuit enabling consumer-oriented systems at Ka band. The integrated components are a preamplifier, a mixer with an IF buffer and a local oscillator. The conversion gain is determined to be 16.3 dB for an intermediate frequency of 100 MHz.**

I. Introduction

In communications systems the allocation of the 24 GHz band for ISM applications is getting more important with increasing introduction of new wireless services, which leads to a rapid increase of spectral congestion at the commonly used frequencies below 6 GHz. Wireless applications at more elevated frequencies did not penetrate the mass market because of cost reasons (with the exception of TV satellite broadcasting at 12 GHz). Unlike at lower frequencies, the analog front-end electronics becomes a major cost factor as the frequency of operation is being increased.

Coplanar and microstrip oscillators operating around 24 GHz have already been reported in [1]. Also a more compact oscillator using lumped elements has been descried in [2]. This paper will demonstrate a fully integrated receiver front-end addressing the ISM band at 24 GHz using HBTs in a commercially available Si/SiGe HBT MMIC process. This is to the best of our knowledge the first SiGe HBT monolithic receiver chip for the 24 GHz ISM band ever reported in the literature.

II. Technological features

The basis for the integrated circuits discussed in this paper is the commercially available Si/SiGe HBT technology at ATMEL Wireless & μC (Heilbronn, Germany). For transistors with the standard 1.2 μm wide emitter structures, f_T = 30 GHz and f_{max} = 50 GHz have been demonstrated. Through different collector doping profiles selectable for each individual transistor by a selective collector implant, the transit frequency can be increased to 50 GHz. Full details of the technology is described in [3] and [4], for instance. For all circuits shown here, standard substrates with a substrate resistivity of 20 Ωcm is used. The transistors with standard 1.2 μm wide emitter structures have been modified by introducing interdigital collector electrodes for multi-emitter-finger structures. This modification is described in [5].

III. Integrated functional blocks

The chip photograph of the fully integrated receive front-end can be seen in Figure 1. The individual circuit parts of the receiver, described and characterized in sections III.A, III.B and III.C, are the preamplifier, voltage controlled oscillator and mixer, respectively. They are also separately realized on the same die with contacts for on-wafer measurement.

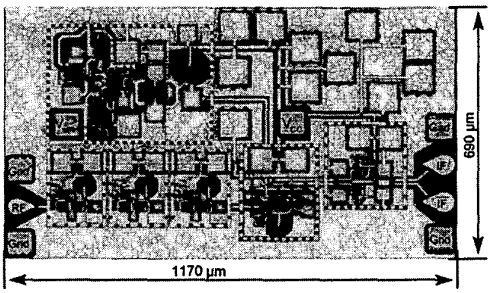

Figure 1: Chip photograph of the receive front-end at 24 GHz

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A. Preamplifier

The preamplifier is a three stage amplifier in cascode configuration, with an identical circuit topology depicted in Figure 2. The current density of the RF transistors $(1 \times 1.2 \times 20\,\mu m^2)$ is set to their f_T-maximum (12 mA). The transistors T1 and T2 are biased by a current mirror and a voltage divider, respectively.

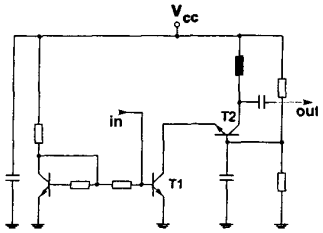

Figure 2: Circuit schematic of a single stage of the preamplifier at 24 GHz. 3 stages are cascaded for the complete preamplifier.

The amplifier in Figure 2 is cascaded in series three times. The chip photograph of the resulting amplifier for 24 GHz is shown in Figure 3.

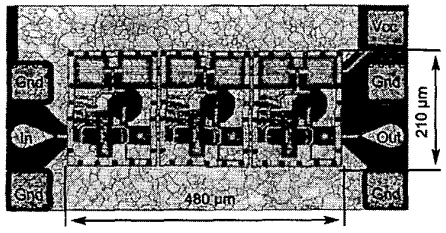

Figure 3: Chip photograph of the three stage preamplifier at 24 GHz

On-wafer S-parameter and noise figure measurements have shown that in a 50 Ω test environment the amplifier provides a maximum gain of 10 dB and a noise figure of 9 dB at 24 GHz. In the frequency region between 23.5 GHz and 24.5 GHz the gain is nearly constant (see Figure 4).

The DC power consumption is 165 mW at a 3.6 V supply voltage.

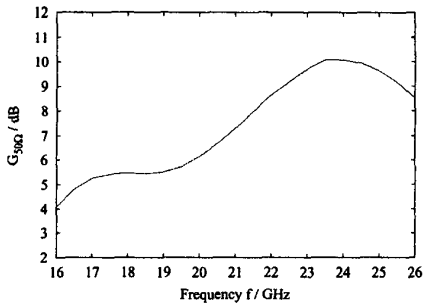

Figure 4: Gain of the preamplifier in a 50 Ω test environment

B. Local oscillator

The design philosophy behind this oscillator is to reduce the consumed chip area to a minimum and provide a load-independent oscillation condition with high output power. A 16 GHz high power ultra compact oscillator design is presented in [5].

By using active reactance concepts, the oscillator core is built up by a parallel resonance circuit, followed by cascode stage buffer amplifier with an on-wafer LC-matching network. In comparison to [6] only the bias current is increased and an on-wafer spiral inductor is added for DC supply.

Figure 5 shows a chip photograph of the realized MMIC prototype. Neglecting the pad configuration, the oscillator is realized on a chip area of $430 \times 320\,\mu m^2$.

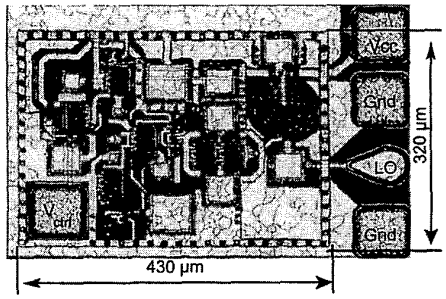

Figure 5: Chip photograph of the VCO at 24 GHz

The spectral output of the VCO can be seen in Figure 6. On wafer phase noise measurements with a

spectrum analyser indicate a value of -83 dBc/Hz at 1 MHz offset from carrier, however it is believed to be dominated by low-frequency pick-up in the DC feed.

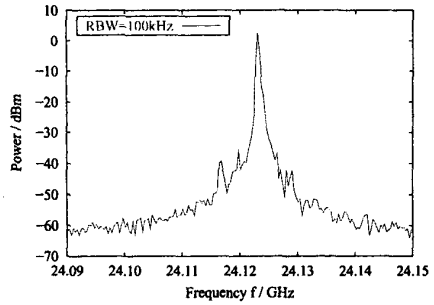

Figure 6: Spectral output of the VCO with an output power of +3 dBm at 24.1 GHz; on-wafer measured phase noise: -83 dBc/Hz at 1 MHz offset

The maximum output power of this VCO is determined to be +3 dBm at 24.1 GHz. The results of the frequency response can be seen in Figure 7.

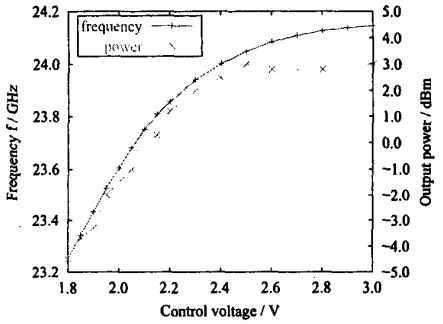

Figure 7: Frequency responce of the VCO

The DC power consumption is 266 mW at a 3.6 V supply voltage.

C. Double balanced mixer

The topology of the mixer is a slightly modified Gilbert cell configuration, followed by an emitter follower buffer stage (see schematic in Figure 8). The mixer is driven single-ended by the RF signal (T1) and the LO signal (T3). The commonly utilized transistor current source for the transistors T1 and T2 is replaced by a spiral inductance of two turns. Lowering the potential levels in the mixer by this replacement increases the linearity of the mixer at the output. The differential IF output of the Gilbert cell is filtered by an RC filter with a corner frequency of 800 MHz and buffered by an emitter follower (T7 and T8), which has a transistor current source as a load.

The DC power consumption is 39 mW at a 3.6 V supply voltage.

IV. System Characteristics

The receiver presented in Figure 1 is characterized on-wafer. The structures at the upper right part of the chip are on-wafer capacitors for DC-blocking purpose.

The conversion gain, shown in Figure 9, is measured single-ended by keeping the IF constant. The LO frequency is set lower than the RF. The highest conversion gain obtained in the single-ended measurement configuration is 13.3 dB. The differential conversion gain of the receiver is then 16.3 dB.

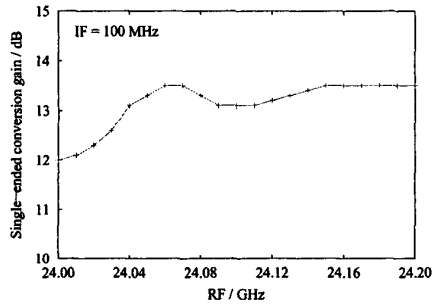

Figure 9: Single-ended conversion gain of the receiver at a constant IF of 100 MHz

In Figure 10 the receiver conversion gain as a function of the RF power is presented. The -1 dB input compression point is determined to be $P_{-1\,\mathrm{dBm,\,in}} = -32.3$ dBm.

The overall DC power consumption is 470 mW at a 3.6 V supply voltage.

V. Conclusion

A standard commercially available Si/SiGe HBT process has been used to fabricate a fully integrated receiver IC for 24 GHz, opening the way to extremely

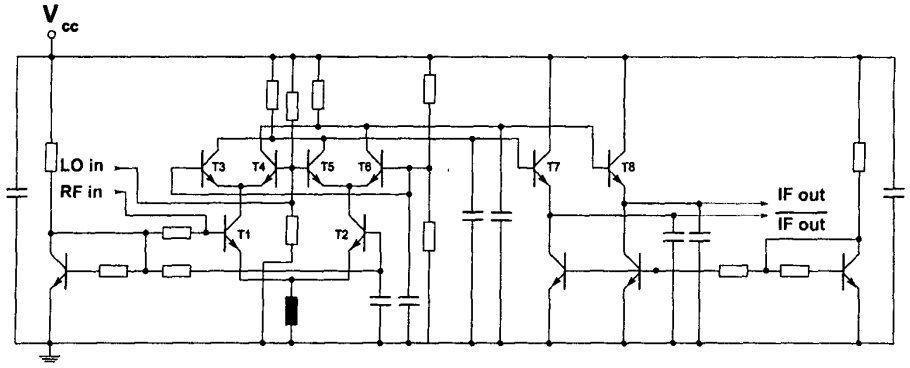

Figure 8: Circuit schematic of the mixer circuit part for 24 GHz

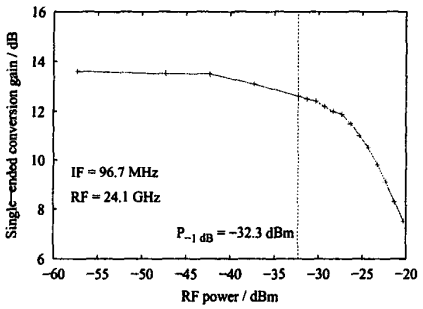

Figure 10: Input -1 dB compression point of the conversion gain at RF=24.1 GHz and IF=96.7 MHz

low cost consumer products in this frequency range, like short-range sensing and wireless communications devices. Further performance enhancements are expected from emerging SiGe HBT processes with improved cutoff frequencies, and from improvements in the passive structures used on the chip.

ACKNOWLEDGMENT

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